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Design and Analysis of a Symmetric 13-Level Multilevel Inverter

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ABSTRACT: Recent progress in power electronic converters has significantly contributed to the evolution of multilevel inverter (MLI) structures. These topologies are widely preferred due to their ability to generate high-quality stepped output waveforms with lower harmonic distortion, reduced device stress, and minimal filtering requirements. In this work, a symmetric source-based 13-level multilevel inverter topology is proposed to achieve an increased number of voltage levels while maintaining a reduced component count. The presented configuration is designed to generate a 13-level staircase output voltage waveform that closely resembles a sinusoidal waveform without adding extra power semiconductor switches. The inverter operates in symmetric mode, where all DC sources have equal magnitude. A Carrier-Based Sinusoidal Pulse Width Modulation (CB-PWM) technique operating at a switching frequency of 3 kHz is employed to control the switching operation. The complete system is modeled and simulated in the MATLAB/Simulink R2019b environment to verify its performance. The study emphasizes the development of a single-phase multilevel inverter capable of producing the maximum possible number of voltage levels using fewer power electronic components. Furthermore, the performance of the proposed 13-level inverter is evaluated at a modulation index of 1 under an RL load condition to analyze its dynamic response and voltage-step generation capability.

I. INTRODUCTION

At present, multilevel inverters (MLIs) have attracted considerable attention in the field of power electronics due to their extensive applications and technical advantages [1]–[3]. Conventional two-level inverters often suffer from poor waveform quality, high switching stress, and electromagnetic interference (EMI) problems [4]. These limitations are significantly mitigated in MLIs, which are capable of generating a high-quality staircase sinusoidal output voltage with reduced total harmonic distortion (THD) [5], [6]. In addition, MLIs minimize switching losses and often eliminate the requirement for bulky external filters [7]. Due to these advantages, MLIs are widely employed in high-voltage DC (HVDC) transmission systems, electric vehicles, and adjustable-speed drive applications [8]–[10]. With the increasing penetration of renewable energy resources, MLIs have become essential in solar photovoltaic (PV) and wind energy conversion systems [11], [12]. Their suitability for medium-voltage and high-power applications makes them highly desirable for modern grid-connected systems [13]. Multilevel inverters are extensively used in renewable energy integration, where they convert DC power from solar panels or wind generators into grid-compatible AC power with improved efficiency and power quality [11], [12]. In motor drive applications, MLIs provide smooth speed and torque control with enhanced efficiency compared to traditional two-level inverters [9], [14]. They are also used in grid-tied inverter systems for distributed energy resources (DERs), enabling reactive power compensation and voltage regulation [15]. In HVDC transmission, MLIs improve long-distance power transfer efficiency and system stability [8], [16]. Furthermore, in electric vehicles (EVs), MLIs convert battery DC power into AC motor drive power and facilitate regenerative braking operations [10], [17]. By utilizing multiple DC voltage sources, MLIs synthesize stepped output voltage waveforms that closely approximate a sinusoidal waveform, thereby reducing THD and dv/dt stress across switching devices [5], [18]. This improves reliability and allows the use of lower-rated semiconductor devices, reducing overall system cost [19]. Historically, several classical MLI topologies have been developed. The flying capacitor (FC) inverter was introduced as an alternative multilevel structure [20]. The neutral point clamped (NPC) inverter, also known as the diode-clamped inverter, was proposed to achieve voltage sharing across switches [21], [22]. The cascaded H-bridge (CHB) inverter was developed to generate stepped output voltages using separate DC sources [23]. These conventional topologies laid the foundation for further research in multilevel converter technology. Despite their advantages, traditional MLIs require a large number of switches, capacitors, and sometimes multiple isolated DC sources, increasing system complexity and cost [24]. To overcome these limitations, several reduced-component and asymmetrical MLI structures have been proposed in recent years to enhance efficiency while minimizing device count [3], [19]. Modern MLIs are broadly classified as symmetrical and asymmetrical based on the magnitude of DC input sources. In symmetrical structures, all DC sources have equal voltage values, whereas asymmetrical configurations use



unequal voltage magnitudes to achieve a higher number of output levels with fewer components [18]. In this study, a symmetrical 13-level MLI configuration is introduced. The effectiveness of the proposed topology is analyzed through MATLAB/Simulink simulations under RL load conditions at modulation index 1. The structure of the paper is organized as follows: Section 3 explains the operating principles and modulation strategy of the proposed inverter; Section 4 details the different operating modes; and Section 5 presents the simulation setup along with the corresponding results and discussion.

II. PROPOSED TOPOLOGY

The proposed symmetric 13-level multilevel MLI is depicted in the Fig.1. The configuration employs a total of eleven power switches, among which T8, T9, T10, and T11 are bidirectional switches, while the remaining switches operate in a unidirectional manner. The bidirectional switches enable proper current flow during different operating modes and facilitate flexible voltage level generation. The topology is composed of two main sections: a level generation unit and a polarity generation unit (H-bridge). The level generation part is responsible for synthesizing the required stepped DC voltage by appropriately connecting or bypassing the equal DC sources. The polarity generation unit, formed by four main switches, produces the positive and negative half cycles of the output voltage without requiring additional DC sources. The inverter operates in symmetric mode, where all DC voltage sources have equal magnitude. By selectively turning ON the appropriate switches, the sources are connected in series to produce different voltage combinations. This arrangement enables the generation of thirteen output voltage levels, including zero level. The symmetric configuration ensures balanced voltage stress across the switches and simplifies modulation and control strategies.

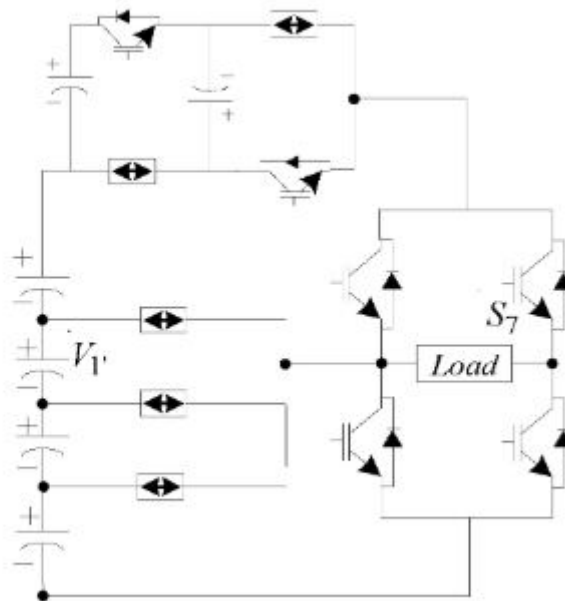
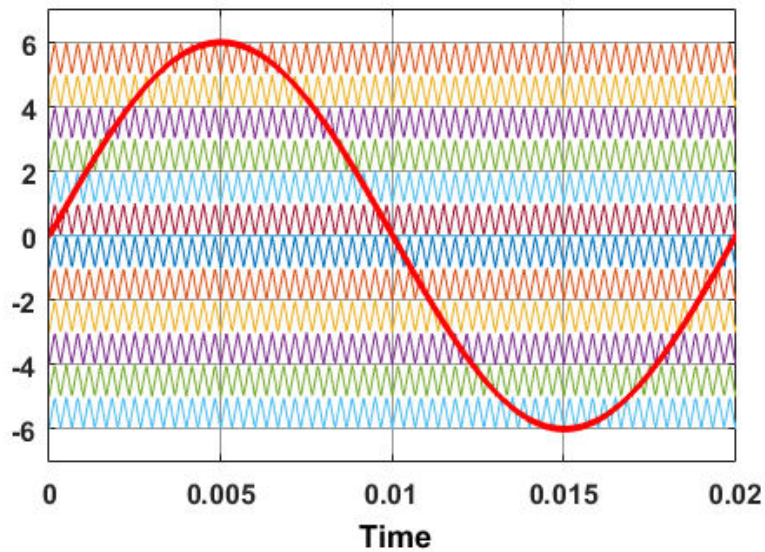


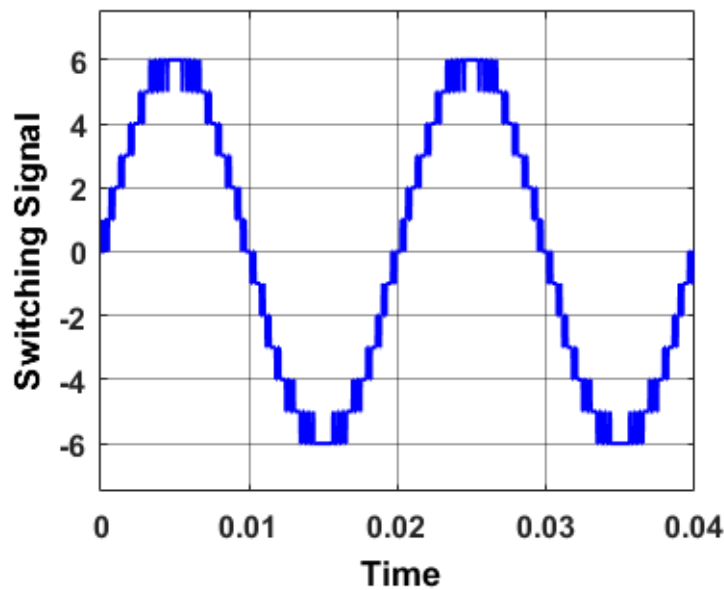
Fig. 1. Proposed MLI topology

III. MODULATION AND CONTROL OF MLI

In the 13-level MLI shown in the fig. 2(a), a low-frequency sinusoidal reference signal is compared with multiple high-frequency triangular carrier waves (twelve carriers for a 13-level output) operating at around 3 kHz. The reference sine wave determines the fundamental output frequency, while its amplitude controls the modulation index and thereby the magnitude of the output voltage. Whenever the sinusoidal reference intersects with any of the carrier signals, switching pulses are generated to control the power semiconductor devices. As the reference waveform moves through the different carrier bands, the inverter switches between several discrete voltage levels, producing thirteen distinct levels (six positive, six negative, and one zero level). This results in a staircase output waveform that closely approximates a sinusoidal shape, significantly reducing total harmonic distortion (THD), minimizing dv/dt stress across the switches, and improving overall output waveform quality. Fig. 2(b) shows the resulting stepped output voltage waveform produced through this switching operation.



(a)



(b)

Fig. 2: Pulse-width modulation process: (a) Reference sine wave compared with carrier signals; (b) Generated switching waveform for the 13-level inverter.

IV. MODES OF OPERATION

The thirteen voltage levels of the proposed inverter are obtained by appropriately selecting specific switch combinations, as listed in Table 1. For each level, the switches marked with a \checkmark are turned ON, while the others remain OFF (\times). The highest positive level, +6Vdc, is produced by turning ON S1, S2, S6, and S7. The +5Vdc level is achieved using S1, S2, S5, and S6, and +4Vdc is generated with S1, S2, S7, and S8. For +3Vdc, switches S2 and S9 are activated, whereas +2Vdc and +1Vdc are obtained by turning ON S2 with S10 and S2 with S11, respectively. The zero level (0Vdc) is formed by switching ON S2 and S4. Similarly, the negative levels are created by reversing the conduction path: -1Vdc is generated with S3, S7, S8, and S9 ON; -2Vdc with S3, S7, S8, and S9; -3Vdc with S3, S7, S8, and S10; -4Vdc with S3, S4, S7, and S8; -5Vdc with S3, S4, S5, and S6; and -6Vdc with S3, S4, S6, and S7. In this way, each of the thirteen output levels is produced through a unique switching state, enabling proper connection of the DC sources to generate the required stepped waveform. The operating modes corresponding to these levels are



depicted in Fig. 3.4, where the green arrow indicates the current flow during the positive half-cycle and the red arrow represents the negative half-cycle conduction path.

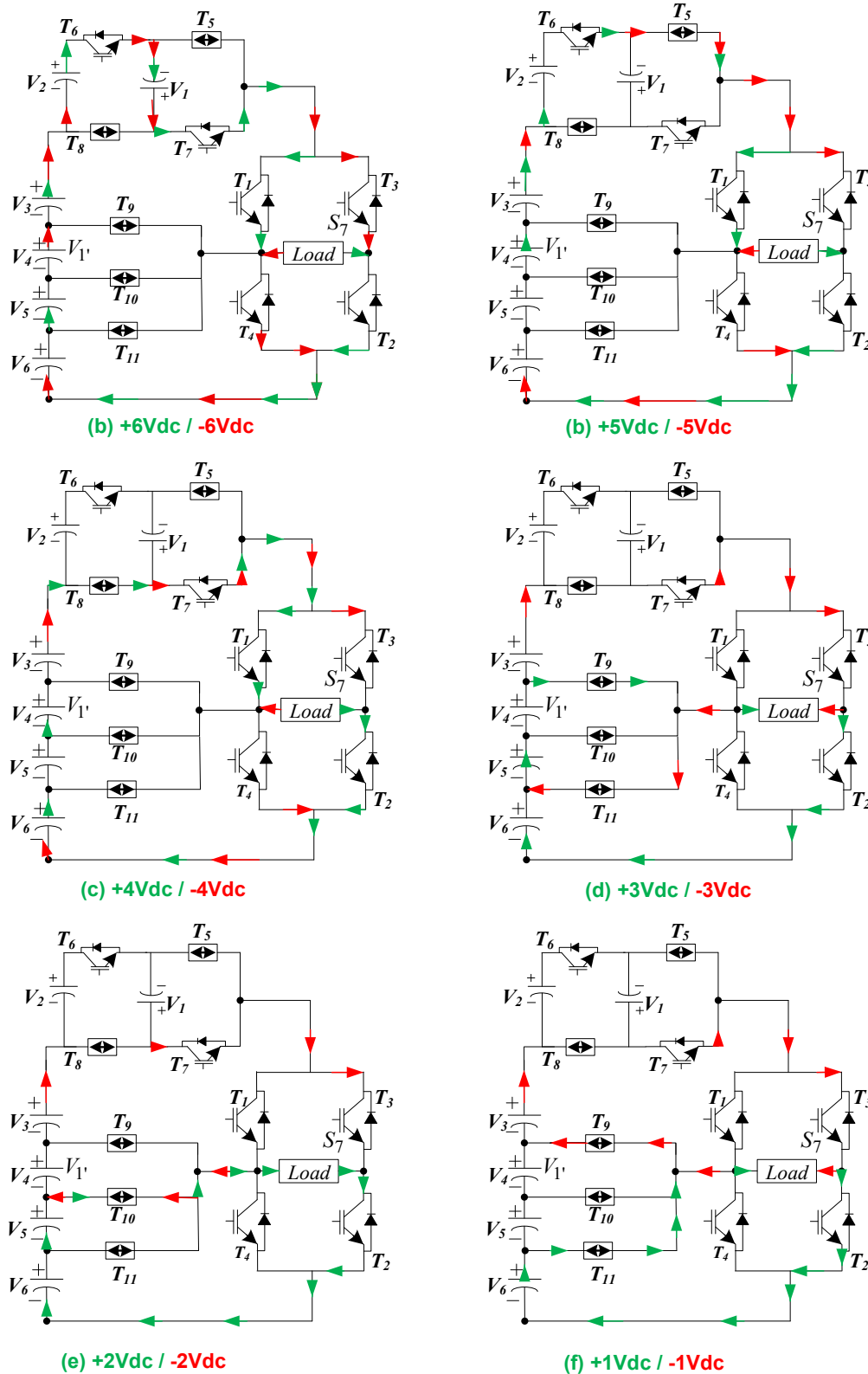


Fig.4. Modes of operation for positive and negative half cycle of the proposed MLI

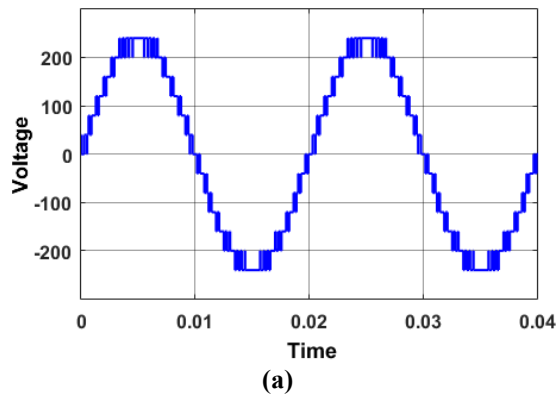


Table. 1. Switching status of proposed MLI

	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁
+6V _{dc}	✓	✓	X	X	X	✓	✓	X	X	X	X
+5V _{dc}	✓	✓	X	X	✓	✓	X	X	X	X	X
+4V _{dc}	✓	✓	X	X	X	X	✓	✓	X	X	X
+3V _{dc}	X	✓	X	X	X	X	X	X	✓	X	X
+2V _{dc}	X	✓	X	X	X	X	X	X	X	✓	X
+1V _{dc}	X	✓	X	X	X	X	X	X	X	X	✓
0V _{dc}	X	✓	X	✓	X	X	X	X	X	X	X
-1V _{dc}	X	X	✓	X	X	X	✓	✓	✓	X	X
-2V _{dc}	X	X	✓	X	X	X	✓	✓	✓	X	X
-3V _{dc}	X	X	✓	X	X	X	✓	✓	X	✓	X
-4V _{dc}	X	X	✓	✓	X	X	✓	✓	X	X	X
-5V _{dc}	X	X	✓	✓	✓	✓	X	X	X	X	X
-6V _{dc}	X	X	✓	✓		✓	✓	X	X	X	X

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the simulation results of the proposed 13-level inverter topology are presented. A detailed model was developed in the MATLAB/Simulink R2019b environment to verify the operational performance of the inverter. A symmetrical DC source configuration is employed, with six DC sources each rated at 40 V (V1 through V6). This equal voltage arrangement facilitates a higher number of output voltage levels, allowing the inverter to generate 13 distinct steps. The system is tested at a modulation index of 1, with an RL load comprising a 50 Ω resistor and a 75 mH inductor. The simulation results indicate a maximum output voltage of 240 V and a peak load current of 1.6 A.



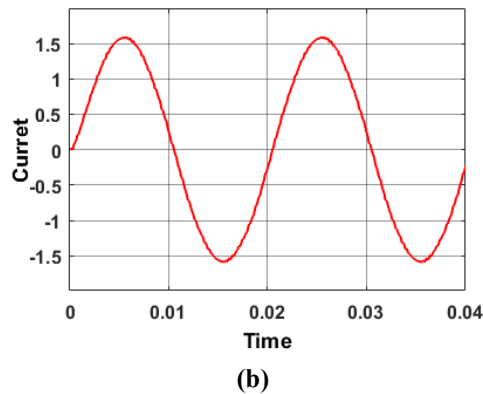


Fig. 4. Simulation results for the (a) output voltage; (b) load current; at MI = 1

V. CONCLUSION

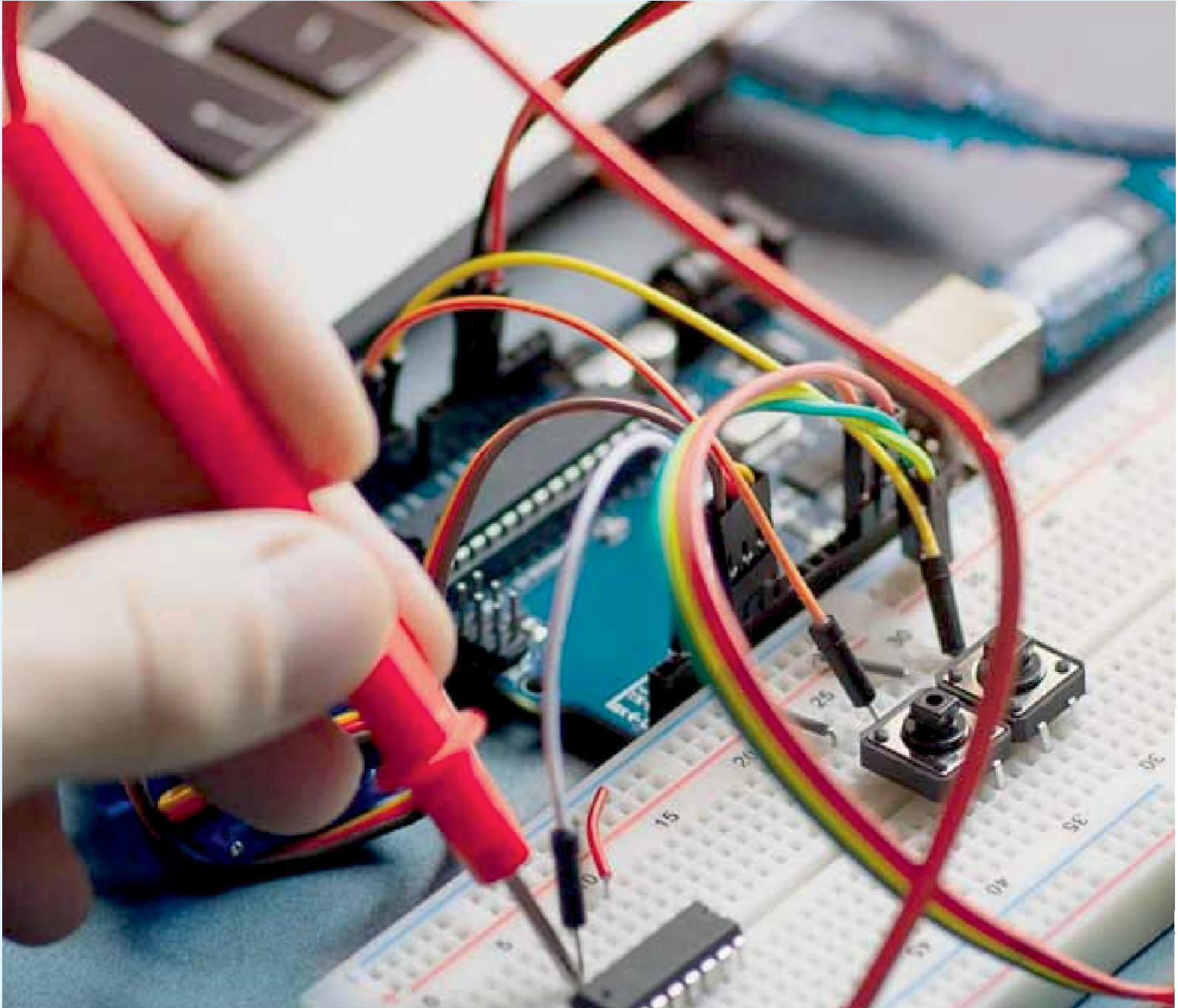
This paper presented a symmetrical 13-level multilevel inverter (MLI) topology with a reduced number of power switches. The proposed configuration utilizes eleven switches, including four bidirectional switches, and is divided into a level generation unit and a polarity generation unit (H-bridge). The symmetric arrangement with six equal 40 V DC sources ensures balanced voltage stress and simplified modulation control. By appropriately switching the sources in series, the inverter successfully generates thirteen distinct voltage levels, including zero, resulting in improved output waveform quality. Simulation studies carried out in MATLAB/Simulink R2019b under RL load conditions (50 Ω , 75 mH) at a modulation index of 1 confirm proper operation. The inverter achieved a maximum output voltage of 240 V and a peak load current of 1.6 A. Overall, the proposed topology offers a compact structure, reduced switch count, and effective voltage level generation, making it suitable for medium-voltage and renewable energy applications.

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